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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No. 09/955,632
Filing Date September 18, 2001
Inventor Kunal R. Parekh et al.
Assignee Micron Technology, Inc.
Group Art Unit 2813
Examiner Unassigned
Attorney Docket No. MI22-1816
Title: Capacitors, DRAM Arrays, Monolithic Integrated Circuits, and Methods of Forming
Capacitors, DRAM Arrays, and Monolithic Integrated Circuits

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APR 10 2002

Assistant Commissioner for Patents
Washington, D.C. 20231

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CERTIFICATE OF FACSIMILE TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that the following papers are being facsimile transmitted to
the Patent and Trademark Office at (703) 872-9318 on the date shown below:

1. Supplemental Information Disclosure Statement
2. PTO Form-1449
3. Two (2) cited references

Dated: April 10, 2002

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Forming Capacitors, DRAM Arrays, and Monolithic Integrated Circuits

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -See Attached Form PTO-1449

The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449, copies of which are attached. No admission is made regarding whether all the submitted references are prior art.

Citation of the referenced art is respectfully requested.

This Supplemental Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing date of a first Office Action, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.

Respectfully submitted,

Dated:



By:


Frederick M. Fliegel, Ph.D.
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